DATA SHEET

74LV139
Dual 2-to-4 line decoder/demultiplexer

Product data
Supersedes data of 1998 Apr 28

2003 Mar 13

Philips
Semiconductors

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Dual 2-to-4 line decoder/demultiplexer 74LV139

FEATURES

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

APPLICATIONS

- Memory decoding or data-routing
- Code conversion

DESCRIPTION

The 74LV139 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT139.

The 74LV139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$).

When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA_n to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$	C_L = 15 pF; V_{CC} = 3.3 V	11 10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per multiplexer	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	42	pF

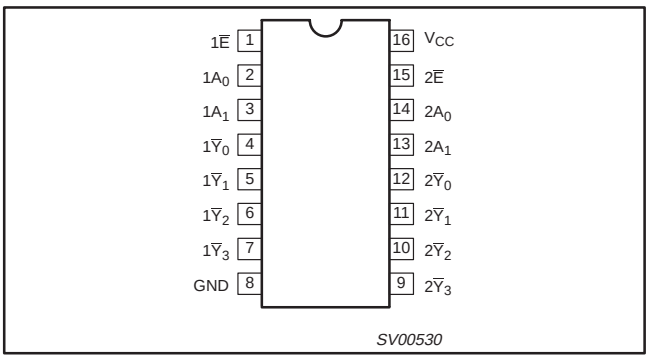
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   N = number of outputs switching;
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	PKG. DWG. #
16-Pin Plastic DIL	–40 °C to +125 °C	74LV139N	SOT38-4
16-Pin Plastic SO	–40 °C to +125 °C	74LV139D	SOT109-1
16-Pin Plastic SSOP Type II	–40 °C to +125 °C	74LV139DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40 °C to +125 °C	74LV139PW	SOT403-1

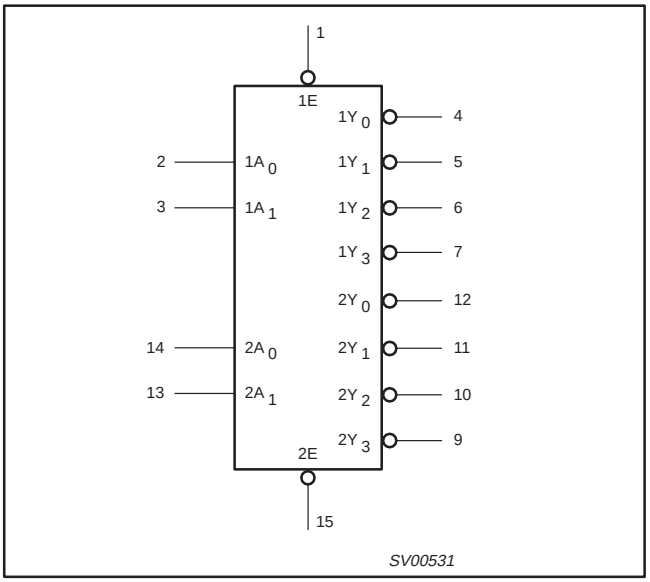
PIN CONFIGURATION



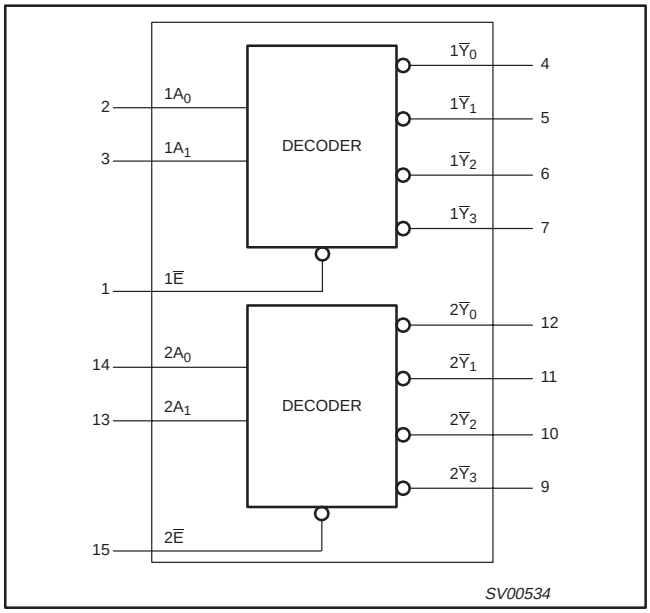
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	Enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	Address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs (active LOW)
8	GND	Ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs (active LOW)
14, 13	$2A_0$, $2A_1$	Address inputs
16	V_{CC}	Positive supply voltage

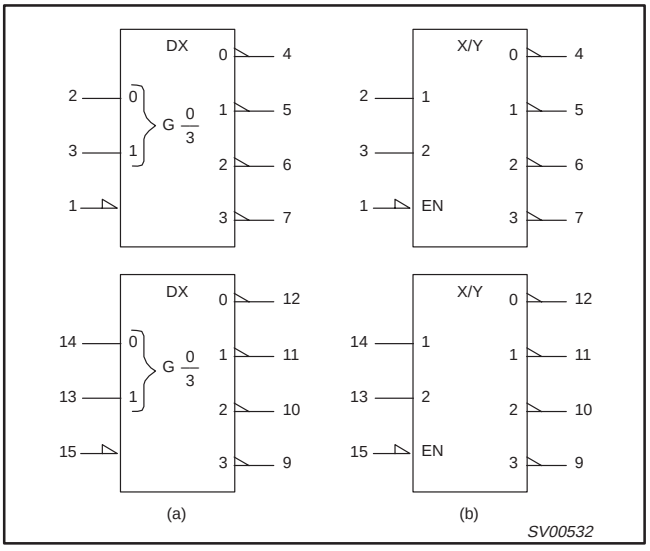
LOGIC DIAGRAM



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V	–	–	500	ns/V
		V_{CC} = 2.0V to 2.7V	–	–	200	ns/V
		V_{CC} = 2.7V to 3.6V	–	–	100	ns/V
		V_{CC} = 3.6V to 5.5V	–	–	50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ V or $V_I > V_{CC}$ + 0.5 V	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ V or $V_O > V_{CC}$ + 0.5 V	50	mA
$\pm I_O$	DC output source or sink current (standard outputs)	-0.5 V < V_O < V_{CC} + 0.5 V	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 °C to +125 °C above +70 °C derate linearly with 12 mW/K above +70 °C derate linearly with 8 mW/K above +60 °C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			–40 °C to +85 °C			–40 °C to +125 °C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 V to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 V to 5.5 V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 V to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 V to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100 µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100 µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100 µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100 µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100 µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6 mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12 mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100 µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100 µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100 µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100 µA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 100 µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6 mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 12 mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ kΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 °C to +85 °C			–40 °C to +125 °C		
			V_{CC} (V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA_n to $\overline{Y}_n$	Figures 1, 2	1.2		70				ns
			2.0		24	31		39	
			2.7		18	23		29	
			3.0 to 3.6		13[2]	18		23	
			4.5 to 5.5			15		19	
t_{PHL}/t_{PLH}	Propagation delay $n\overline{E}$ to $\overline{Y}_n$	Figures 1, 2	1.2		60				ns
			2.0		20	27		34	
			2.7		15	20		25	
			3.0 to 3.6		11[2]	16		20	
			4.5 to 5.5			13		16	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25$ °C.
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6 V;
$V_M = 0.5\ V \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

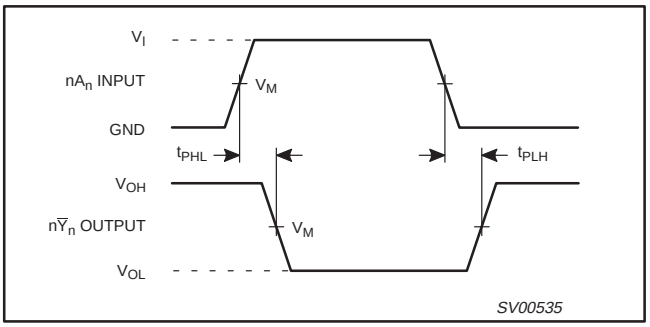


Figure 1. Address input (nA_n) to output ($n\overline{Y}n$) propagation delays.

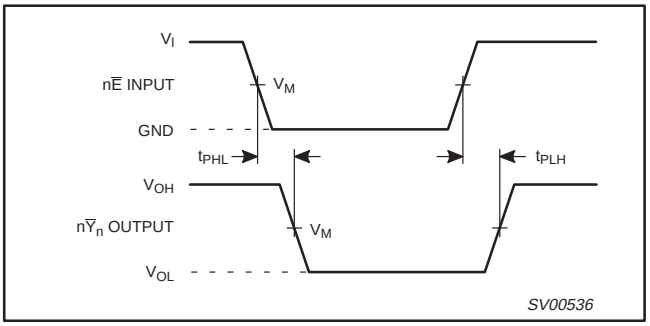
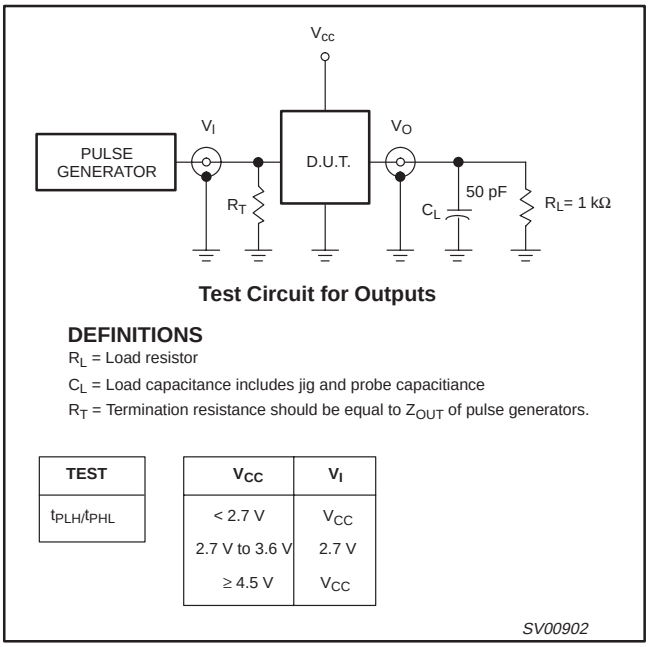


Figure 2. Enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

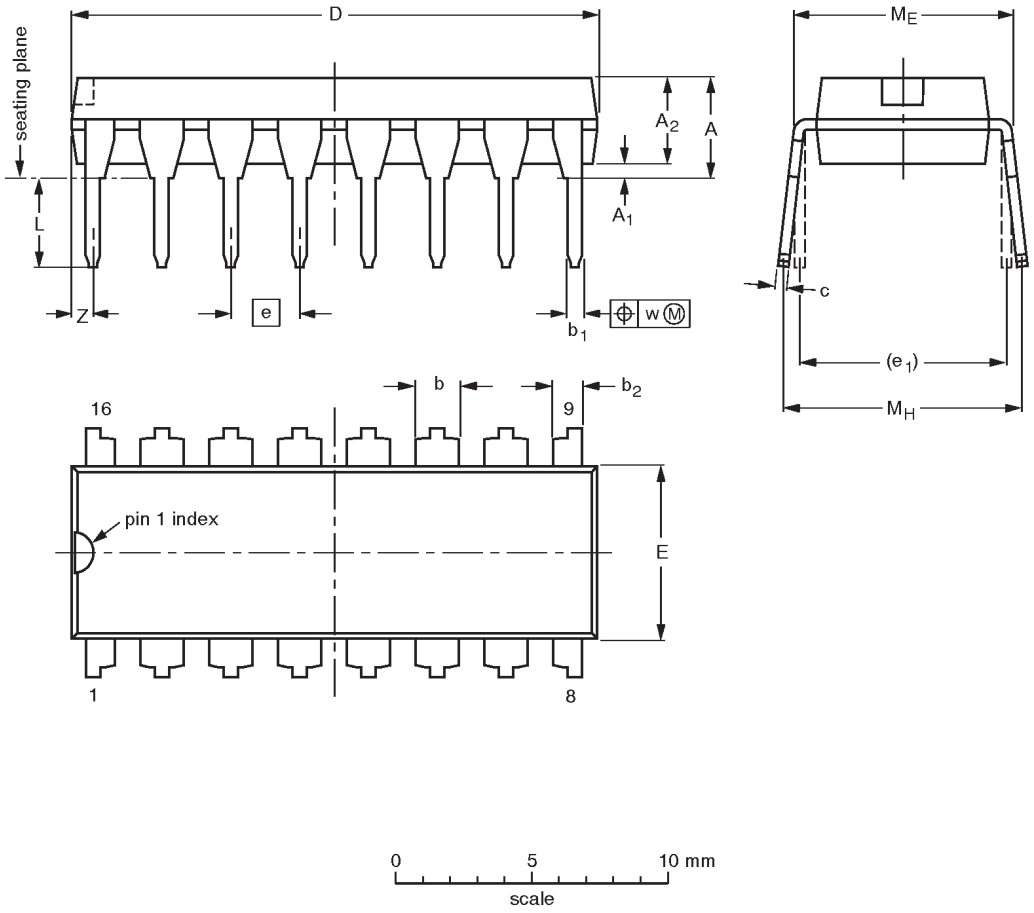
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 V to 3.6 V	2.7 V
≥ 4.5 V	V_{CC}

Figure 3. Load circuitry for switching times.

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

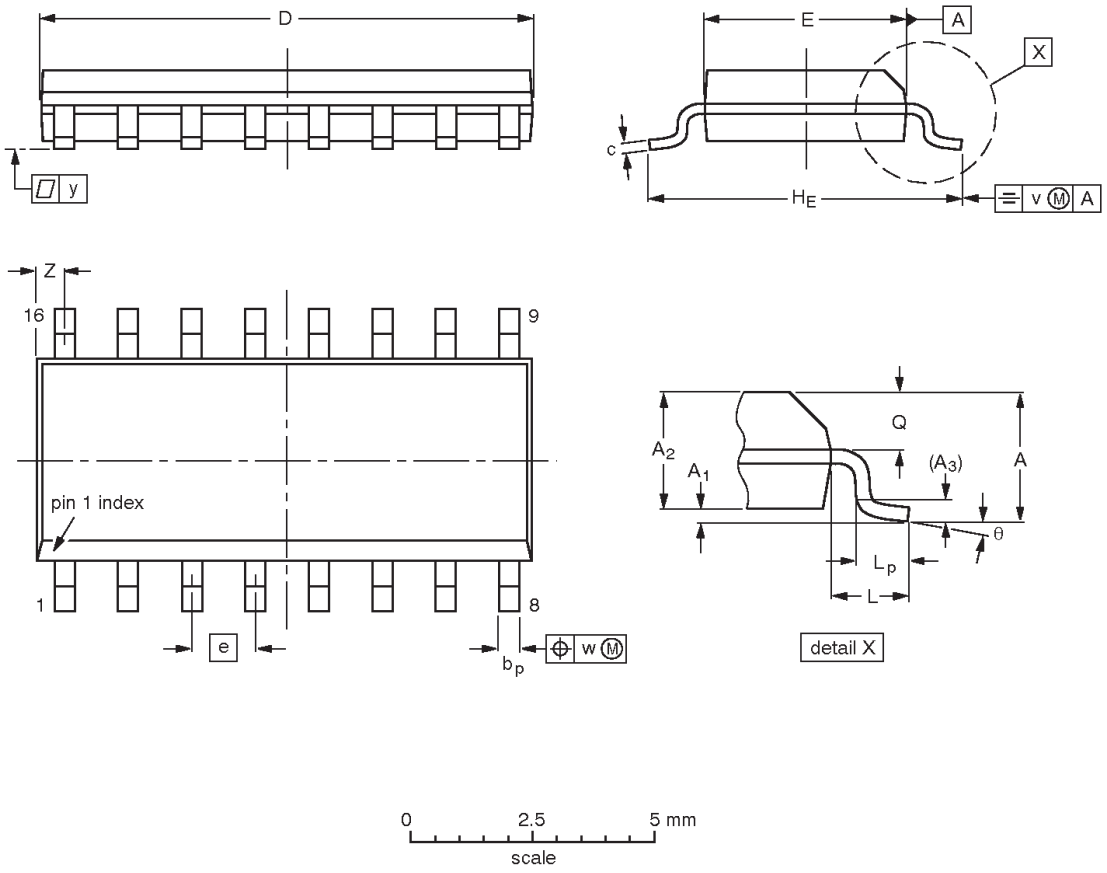
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

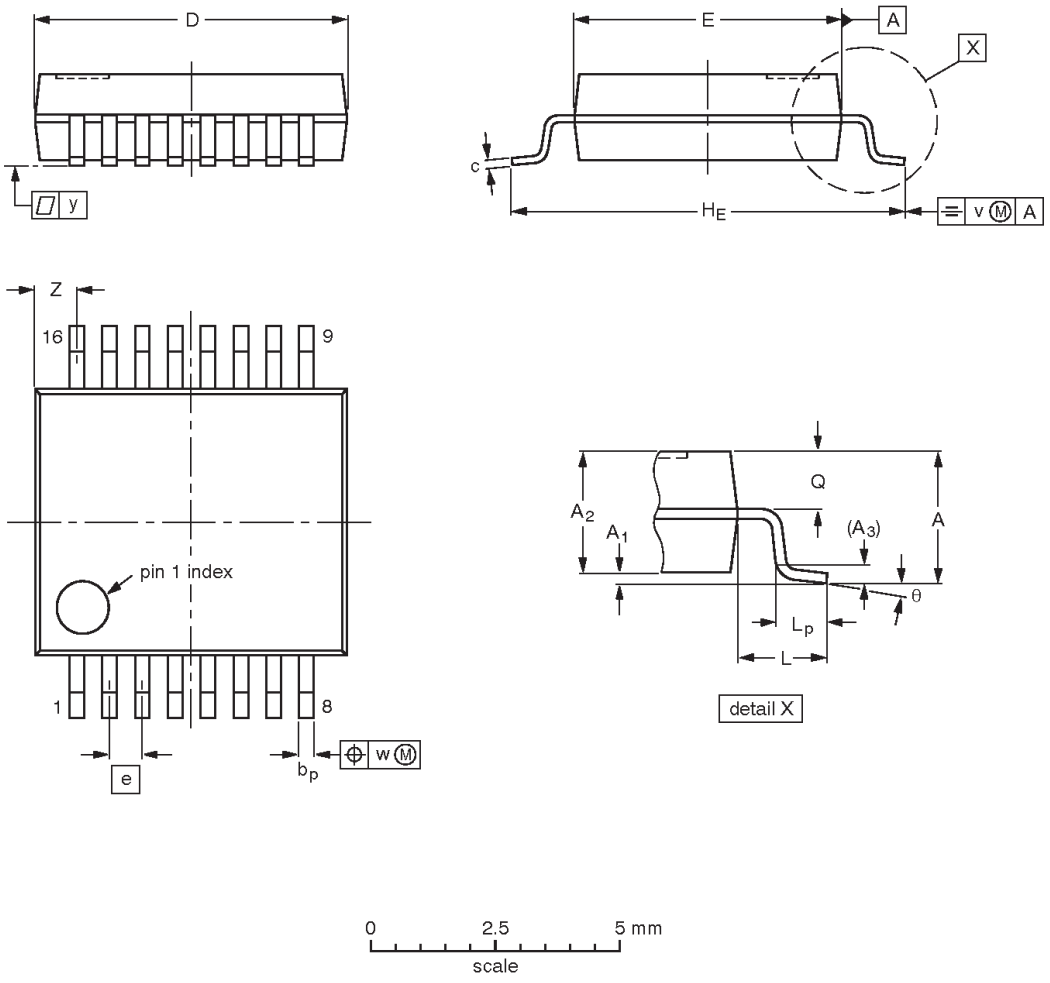
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

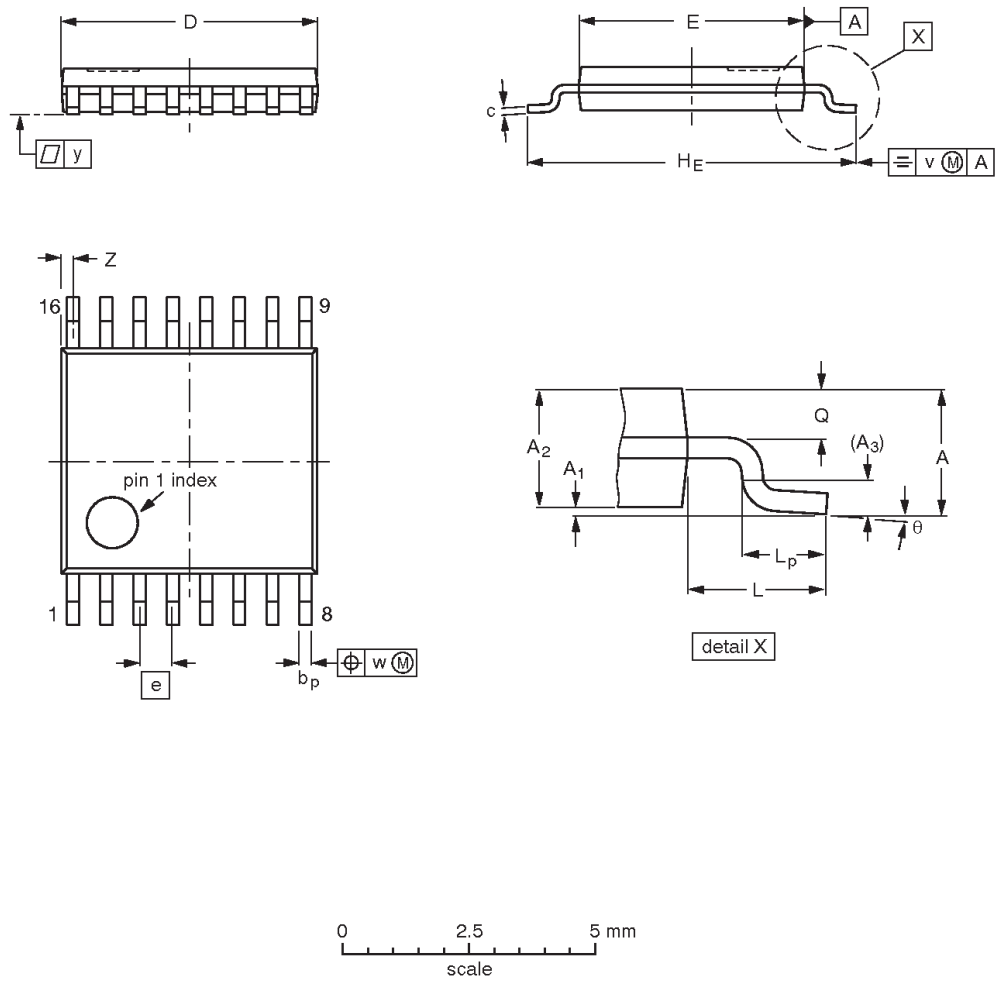
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20030313	**Product data (9397 750 11245). ECN 853-1922 29492 of 07 February 2003. Supersedes Product specification of 1998 Apr 20 (9397 750 04424).** Modifications: ● Quick Reference Data: Correct power dissipation formula in Note 1. ● Ordering information: delete “North America”column; rename column from “Outside North America” to “Order Code”. ● Pin configuration diagram: correct pin number labels .
_2	19980428	**Product specification (9397 750 04424). ECN 853-1922 19290 of 28 April 1998. Supersedes data of 1997 Feb 12.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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